

Dr inż. Daniła Gorodecki, Instituto de Engenharia de Sistemas e Computadores - Investigação e Desenvolvimento (INESC-ID), University of Lisbon

Arithmetic units design based on Boolean representations

The report is dedicated to logic design of arithmetic units from the point of view of Boolean functions implementation. We will consider disjunctive normal form and polynomial expansions, symmetric features of Boolean functions, two- and multilevel minimisations. We will consider some alternative architectures of arithmetic units. Finally we will discuss results of experiments on FPGA and ASIC.