

Dr inż. Daniła Gorodecki

Instituto de Engenharia de Sistemas e Computadores – Investigação e Desenvolvimento (INESC-ID), University of Lisbon

Efficient design of combinational units on FPGA

The report is dedicated to the design of combinational (memory-free) units. We will consider Boolean functions representations in the context of the implementation on FPGA and its features. We will discuss points of collaboration in the field of the arithmetic units design for various areas of the implementation.